VW – (a forward biased breakdown voltage of silicon) [>] VS

where VW is a substrate voltage of a substrate region directly under a gate insulating film and VS is a source voltage of the source offset region, and thereby a resistance value of the source offset region is set independently of a resistance value of the drain offset region in such a manner as to maintain a high sustaining breakdown voltage of the high-voltage MOS transistor, which is based on a voltage of the source offset region and a voltage of the substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor. --

REMARKS

The Examiner's Office Action dated December 3, 2002 has been received and its contents carefully noted. The Applicants respectfully submit that this response is timely filed and fully responsive to the Office Action. The Examiner's indication that claim 5 would be allowable if properly amended to include the features of independent claim 1 and any intervening claims is greatly appreciated. Consequently, claim 5 has been amended to be placed into proper independent form, new claims 12-14 have been added, and claims 1-4 and 7 have been canceled. Therefore, claims 5 and 8-14 are currently pending with claims 8-11 being withdrawn as being directed to a non-elected invention.

With regard to the Examiner's rejections of:

> Claim 1, under 35 U.S.C. 102(a), as being anticipated by the teachings of the Admitted Prior Art (Fig. 13d, 14(a), 14(b), and
>
> Claims 2-4 and 7, under 35 U.S.C. 103(a), as being obvious in view of the teachings of the Admitted Prior Art (Fig. 13d, 14(a), 14(b) combined with the teachings of Yoshihisa (JP '573),

each of these rejections is respectfully traversed.

With regard to the §102(a), the cancellation of claim 1 by the above amendments renders this rejection moot.

The presently claimed invention of independent claims 5 and 12 recite a high-voltage MOS transistor structure in which the dopant concentration of the source

offset region is set lower than that of the drain offset region so as to obtain the high sustaining breakdown voltage, as discussed in Embodiment 2, pages 26-30, and Figures 4, 5 and 6(a)-(d). Additionally, independent claims 13 and 14 recite a high-voltage MOS transistor structure in which the length of the region overlapping between the source offset region and the source well offset region is smaller than that of a region overlapping between the drain offset region and the drain well offset region so as to obtain the high sustaining breakdown voltage, as discussed in Embodiment 3, pages 34-39, and Figures 7, 8 and 9(a)-(d), elements Os and Od.

In contrast to these structures, Yoshihisa (Figure 1) appears to teach the length of the source offset region (see element Ls of Figures 1, 4, 7 of the present application) can be longer than the length of the drain offset region (see element Ld of Figures 1, 4, 7 of the present application) while the reference is silent as to the concentration of the dopant in the source offset region being set lower than that of the drain offset region so as to obtain the high sustaining breakdown voltage.

Additionally, the Admitted Prior Art (Figures 11, 12 and 13(a)-(d)) teaches a high-voltage MOS configuration in which the length of the region overlapping between the source offset region and the source well offset region, Os, is equal of a region overlapping between the drain offset region and the drain well offset region, Od, so as to obtain the high sustaining breakdown voltage, as discussed in pages 2-4, and Figures Figures 11, 12 and 13(a)-(d), elements Os and Od. The Admitted Prior Art does not teach the concentration of the dopant in the source offset region being set lower than that of the drain offset region so as to obtain the high sustaining breakdown voltage.

Since neither the Admitted Prior Art or Yoshihisa teach or suggest the specific dopant concentrations set forth in independent claims 5 or 12, nor do the references specifically teach or suggest the overlap lengths, Os or Od, set forth claims 13 or 14, the rejection, under §103, over the combination of the Admitted Prior Art and Yoshihisa fails to establish a *prima facie* case of obviousness with regard to the

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presently claimed invention. Therefore, it is respectfully requested that the §103 rejection be withdrawn.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,

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MARKED UP VERSION OF AMENDED CLAIMS

IN THE CLAIMS:

Please cancel claims 1-4 and 7.

Please amend claim 5 as follows:

5. (Twice Amended) [The transistor of Claim 2,] A high-voltage MOS transistor wherein a dopant concentration of a [the] source offset region is set lower than a dopant concentration of a [the] drain offset region and thereby a resistance value of the source region is set independently of a resistance value of the drain region in such a manner as to maintain a high sustaining breakdown voltage of the high-voltage MOS transistor, which is based on a voltage of the source offset region and a voltage of a substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.